IN THE CLAIMS

All currently pending claims 1-17 and status identifiers are set forth below.

1. (Original) A computer system comprising:

a host controller;

a first processor bus coupled between the host controller and a first processor;

a second processor bus coupled between the host controller and a second processor;

a random access memory (RAM) coupled to the host controller via a memory bus, the RAM comprising a portion of static memory and a portion of dynamic memory; and

a coherency control module operably coupled to the first processor bus and the second processor bus and comprising:

a request module configured to receive requests from the first processor bus and the second processor bus and to maintain proper ordering of the requests from each processor bus;

an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests currently being processed and to prevent simultaneous multiple accesses to a single address in the static portion of the RAM; and

a static RAM interface module configured to access an address look-up table corresponding to data stored in the static portion of the RAM.

2. (Original) The computer system, as set forth in claim 1, comprising an input/output (I/O) bus coupled between the host controller and a plurality of I/O devices, wherein the I/O bus is operably coupled to the coherency control module and wherein the request module is configured to receive requests from the I/O bus.

3. (Original) The computer system, as set forth in claim 1, wherein the coherency control module is located within the host controller.

4. (Original) The computer system, as set forth in claim 1, wherein the coherency control module comprises a plurality of list structures corresponding to the first processor bus and the second processor bus.

5. (Original) The computer system, as set forth in claim 4, wherein the list structures comprise two-dimensional doubly-linked lists with head and tail pointers.

6. (Original) The computer system, as set forth in claim 5, wherein the list structures comprise dependency links.

7. (Original) The computer system, as set forth in claim 4, wherein the request module comprises a plurality of bypass paths configured to provide a direct request path from the first and second processor buses to the static RAM interface module, thereby bypassing the list structures.

8. (Original) The computer system, as set forth in claim 1, wherein the active snoop queue module comprises a plurality of active snoop queues, each active snoop queue

configured to maintain a list of requests currently being processed and to function independently with respect to each other.

9. (Original) The computer system, as set for the in claim 1, wherein the static RAM interface module comprises a plurality of static RAM interfaces, each static RAM interface corresponding to a segment of the static portion of the RAM.

10. (Original) A coherency control module configured to control access to cache memory in a computer system, the coherency control module comprising:

a request module configured to receive requests from a plurality of buses in a computer system and to maintain proper ordering of the requests from each bus;

an active snoop queue (ASQ) module coupled to the request module and configured to maintain a list of requests from all of the buses currently being processed and to prevent multiple accesses to a single address in the cache memory simultaneously; and

a static RAM interface module configured to access an address look-up table corresponding to data stored in the cache memory.

11. (Original) The coherency control module, as set forth in claim 10, wherein the plurality of buses comprise processor buses.

12. (Original) The coherency control module, as set forth in claim 10, wherein the coherency control module comprises a plurality of list structures corresponding to the first processor bus and the second processor bus.

13. (Original) The coherency control module, as set forth in claim 12, wherein the list structures comprise two-dimensional doubly-linked lists with head and tail pointers.

14. (Original) The coherency control module, as set forth in claim 13, wherein the list structures further comprise dependency links.

15. (Original) The coherency control module, as set forth in claim 12, wherein the request module comprises a plurality of bypass paths configured to provide a direct request path from the first and second processor buses to the static RAM interface module, thereby bypassing the list structures.

16. (Original) The coherency control module, as set forth in claim 10, wherein the active snoop queue module comprises a plurality of active snoop queues, each active snoop queue configured to maintain a list of requests currently being processed and to function independently with respect to each other.

17. (Original) The coherency control module, as set forth in claim 10, wherein the static RAM interface module comprises a plurality of static RAM interfaces, each static RAM interface corresponding to a segment of the static portion of the RAM.